STM32 F0 Series

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STM32 F0 Series: Key Features

Real-time performance

Cortex

48 MHz/38 DMIPS,
5 channels DMA
mapped on 11 IPs +
Bus Matrix allows Flash
execution in parallel with
DMA transfer

Power efficiency

5 µA in Stop mode
2 µA in standby mode
0.4 µA Vbat with RTC,
1.8 V or 2…3.6 V supply,
Fast wake-up time

Superior and innovative peripherals

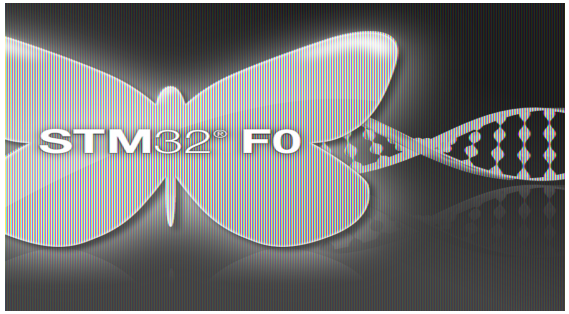
1Mbps I²C Fast mode+
SPI with
4- to 16-bit data frame,
HDMI CEC,
16-bit 3-phase MC timer

Maximum integration

Calendar RTC with
independent supply,
battery backed RAM,
separate analog supply,
safety

Extensive tools and software

ARM + ST ecosytem
(eval board, discovery,
SW library)



STM32 F0 series

L1, F0, F1, F2, F4 series: seamless migration amongst 300 pin-to-pin compatible part #s

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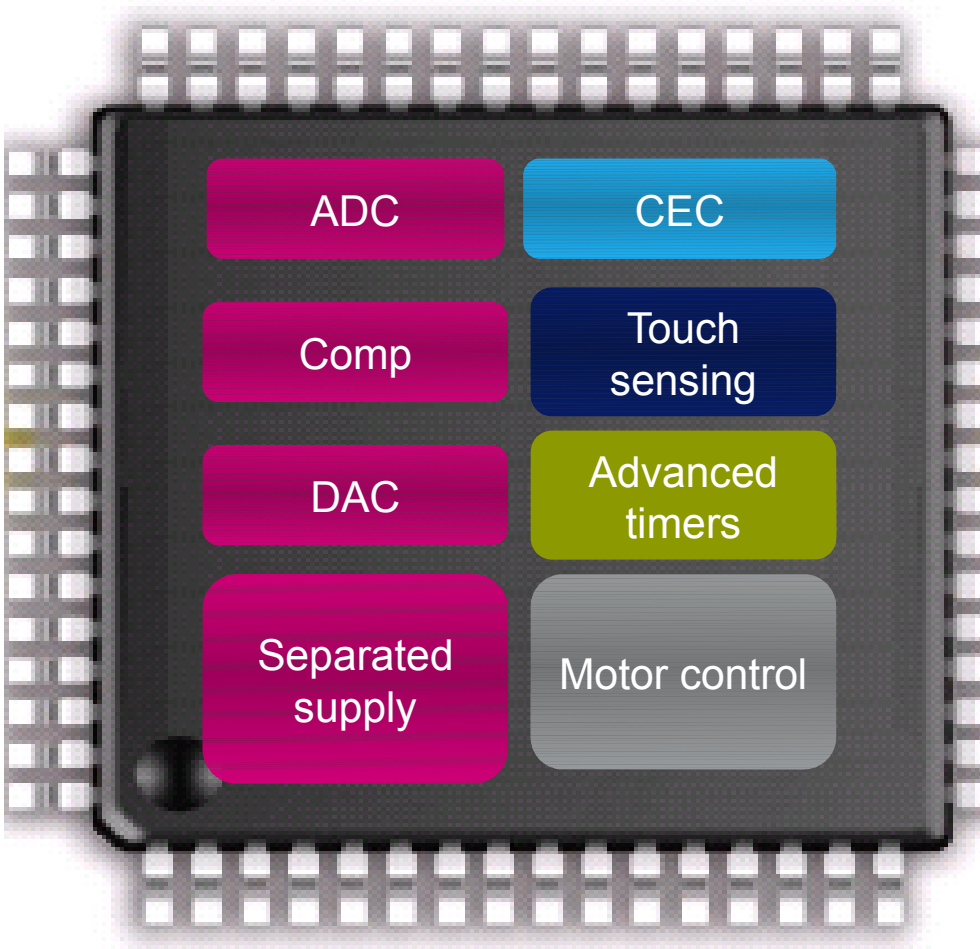
STM32 F0 STM32 DNA

Power Efficiency

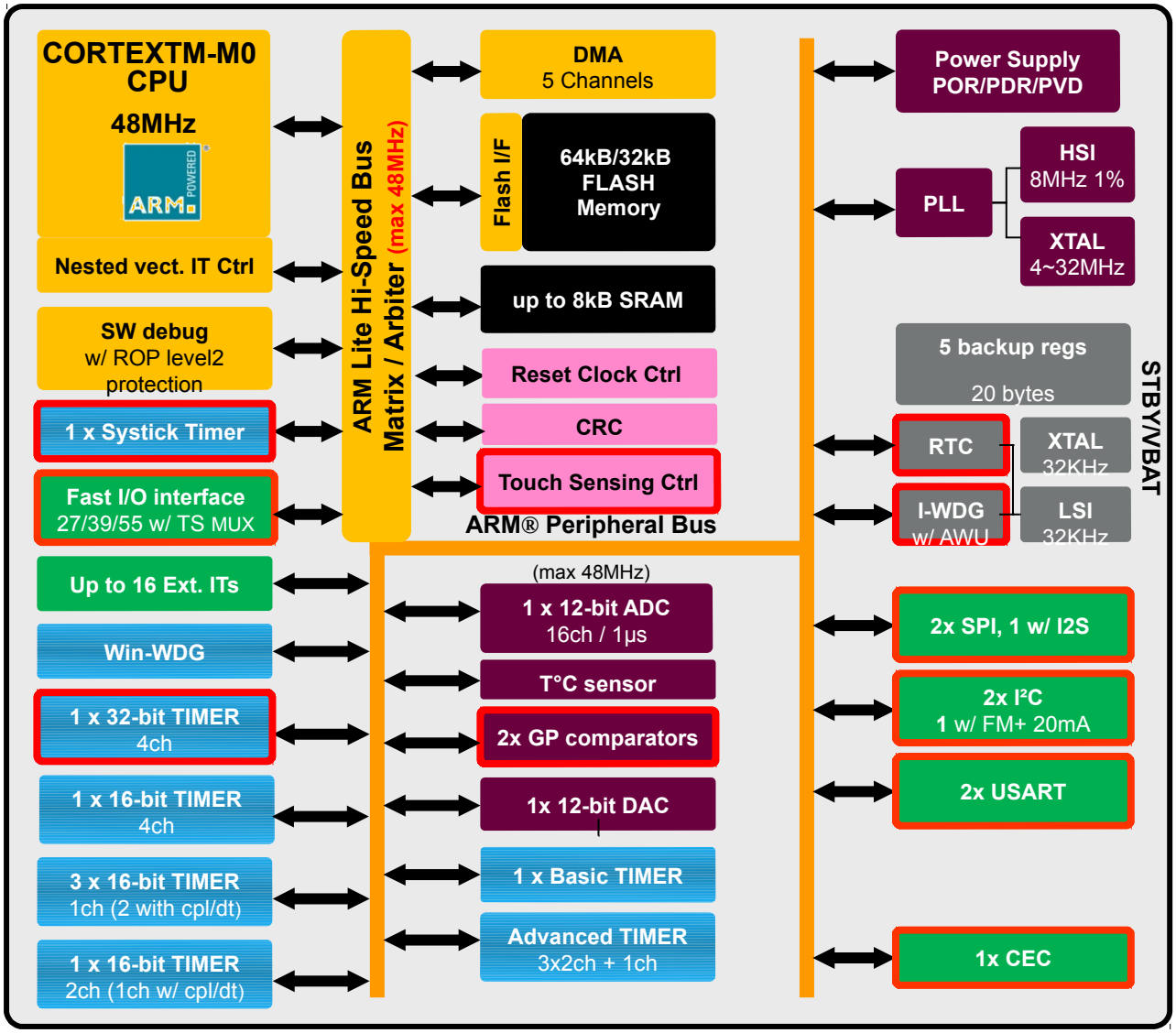
Features	Benefits
Optimized clock system • Integrated clock system with RC calibration • Independent ADC clock source • Communication peripherals with multiple clock sources	**Save cost and power consumption with optimum performance** • Maximum ADC conversion speed • Optimum ADC conversion speed in all circumstance • Communication baud rate independent from CPU frequency and wake-up capability
VBAT • 20 bytes backup registers • 0.43 µA Standby mode combined with RTC	**Lowest current consumption** • Preserved system key variables in Standby mode • Keep track of clock time
RTC • Calendar in BCD format • Prescaler (sub-seconds) in binary format • Calibration trimming • Configurable window / step for final calibration check on customer line • Automatic correction using mains zero-crossing (50 or 60 Hz)	**Accuracy** • Sub-second alarm – 31µs step possible (best fit for RF applications) • Sub ppm RTC • Window : 8s/16s/32s • Step : 3.81ppm/1.91ppm/0.95ppm

Innovative Peripherals

- Analog
  - 12 bit ADC with 1MSPS
  - 12 bit DAC
  - 2x Comparators
  - Separate supply for improved accuracy
- HDMI Consumer Electronics Control (CEC)
- Touch-sensing
  - Up to 18 keys
  - Key, slider and wheel
- Advanced timers
  - 32-bit and 16-bit PWM timers with 17 capture/compare input/outputs mapped on up to 28 pins
- Motor control
  - Permanent Magnet Synchronous Motors (PMSM)



STM32 F0 Block Diagram



→ More in details

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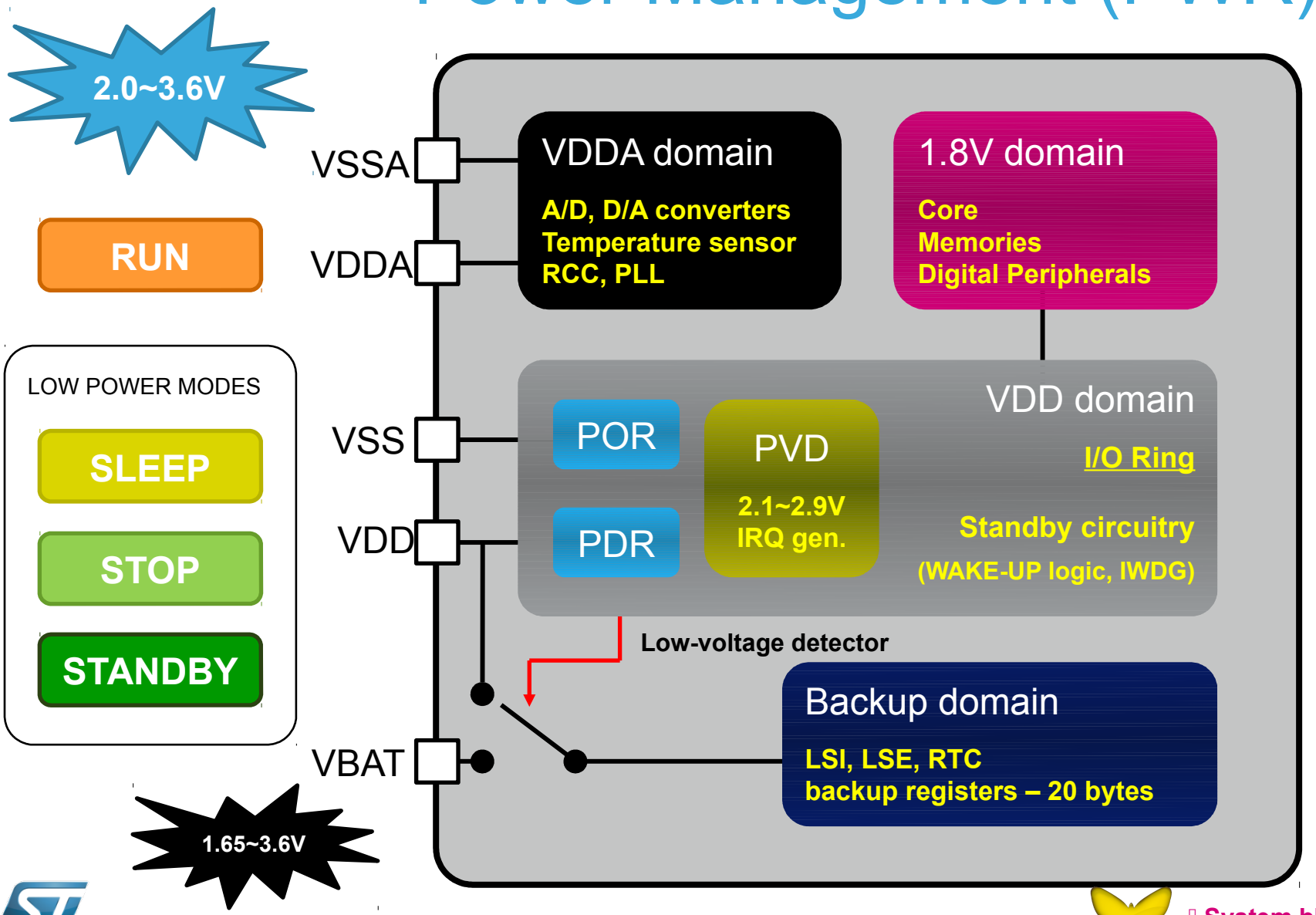
Power Management (PWR)



Low Power Modes

- STM32F05x Low Power modes uses Cortex-M0 Sleep modes

POWER MODE	CONFIGURATION	typical IDD/IDDA *
RUN	@48MHz (HSE bypass 8MHz x 6 PLL = 48MHz)	**22.9 / 0.166 (mA)**
	@24MHz (HSE bypass 8MHz x 3 PLL = 24MHz)	11.7 / 0.088 (mA)
	@8MHz (HSI)	4.15 / 0.079 (mA)
SLEEP	@48MHz (HSI 8MHz / 2 x 12 PLL = 48MHz)	12.9 / 0.243 (mA)
STOP	Voltage Regulator in low power All oscillators OFF, PDR on VDDA is OFF	3.6 / 1.34 (µA)
STANDBY	LSI and IWWDG OFF PDR on VDDA is OFF	**1.1 / 1.21 (µA)**

*)Typical values are measured at TA = 25 °C, VDD =3.3V VDDA= 3.3 V.

In RUN and SLEEP mode, code executed from internal FLASH and all peripherals clock ON.

Reset and Clock Control (RCC)

- System Clock (SYSCLK) sources:
  - **HSE** (High Speed External osc) 4MHz to 32MHz, can be bypassed by user clock
  - **HSI** (High Speed Internal RC): factory trimmed internal RC oscillator 8MHz +/- 1%
  - **internal PLL** x2, x3, .. x16 (16MHz min. output freq.)
- Additional clock sources:
  - **LSI** (Low Speed Internal RC): ~40kHz internal RC
  - **LSE** (Low Speed External oscillator): 32.768kHz, can be bypassed by user clock
  - configurable driving strength (power/robustness compromise)
  - **HSI14** (High Speed Internal RC 14MHz): dedicated oscillator for ADC
- Clock-out capability on the MCO (HSI14, LSI, LSE, SYSCLK, HSI, HSE, PLL/2)
- Clock Security System (CSS) to switch to backup clock in case of HSE clock failure
  - Enabled by SW w/ interrupt capability linked to Cortex NMI
- RTC Clock sources: LSE, LSI and HSE clock divided by 32
- USART, I2C & CEC have multiple possible clock sources

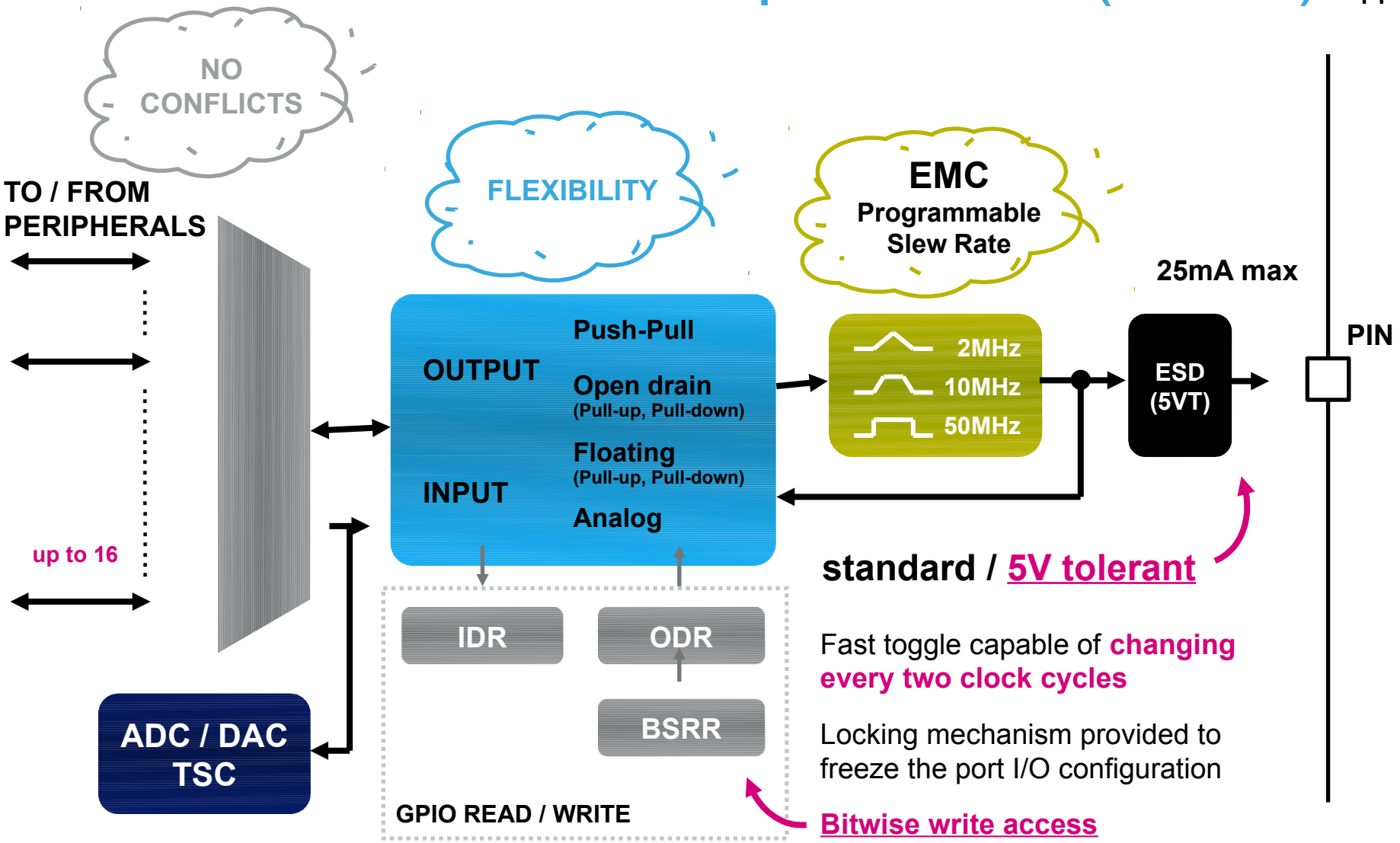
FLASH

- Flash general features:
  - Up to **64KBytes** (64 x 1KBytes page and 16 Sectors of 4KBytes size (4 pages))
  - Endurance: **10k cycles**
  - Access time: **35ns**
  - Half word (16-bit) program time: **52.5µs** (Typ)
  - Page erase time and Mass erase time: 20ms (Min), 40ms (Max)
- Flash interface features:
  - Option Bytes loader
  - Flash program/erase operations
  - **Readout Protection:** Level 0, Level 1 and Level 2 (No debug)
  - **Write Protection**
- Memory organization:
  - Main Program memory block (or Main Flash memory)
  - Information block : 3KBytes of System memory + 6 Option Bytes **(2 for user data)**

Extended Interrupts and Events Controller (EXTI)

- Support generation of up to **28 event/interrupt** requests
- Independent configuration of each line as an external or an internal event requests
- Independent mask on each event/interrupt line
- Possible **automatic disable** of internal lines **when** system is **not in STOP** mode
- Independent trigger for external event/interrupt line
- Dedicated status bit for external interrupt line
- Emulation for all the external event requests

General-Purpose I/Os (GPIO)

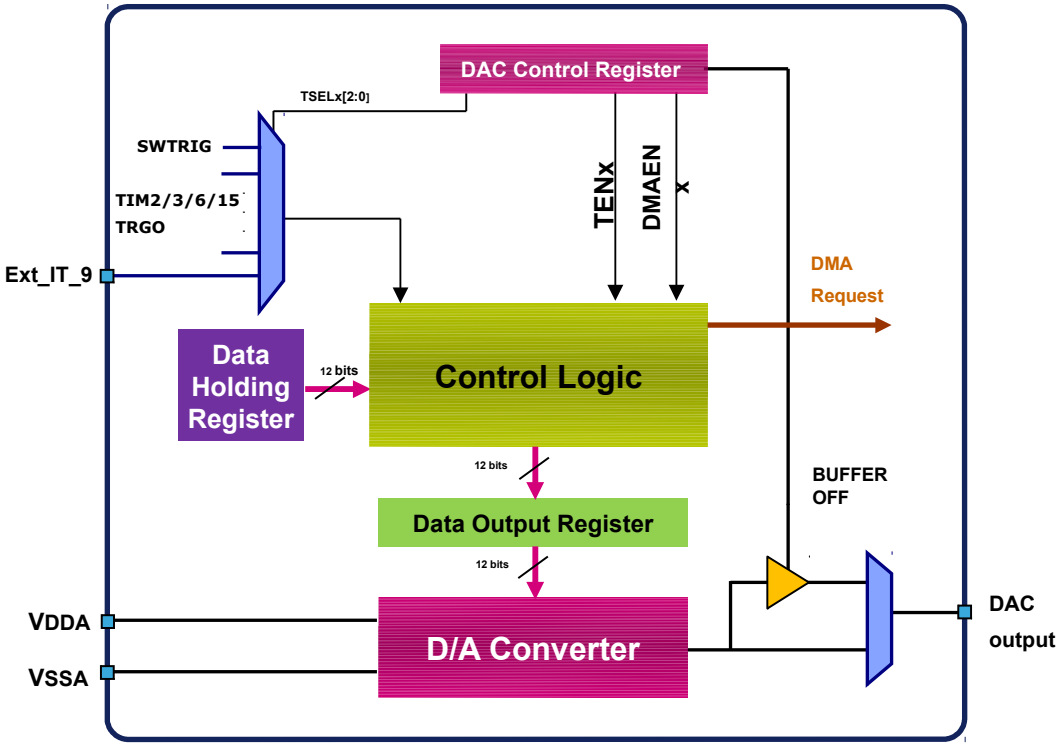


Analog to Digital Converter (ADC)

- ADC conversion rate up to **1 MHz** and **12-bit resolution**
- Programmable Conversion resolution : 12, 10, 8 or 6 bit
- (Conversion range: 0 to VDDA)
- **Up to 19** multiplexed channels (3 internal: **VBAT**, VREFINT, VSENSE)
- Programmable sampling time, single, continuous and discontinuous conversion modes with SW or HW start of conversion (Auto Delay)
- **Self-calibration** and **Auto-OFF** mode for Power Saving
- Configurable scanning direction and data alignment with inbuilt data coherency
- **Analog Watchdog** on high and low thresholds
- DMA capability, Interrupt generation

Digital to Analog Converter (DAC1)

- One single channel DAC with **8-bit or 12-bit** monotonic output
- (Left or right data alignment in 12-bit mode)
- Synchronized update capability
- **DMA capability**
- DMA underrun error detection
- **External triggers** for conversion
- Programmable **internal buffer**
- (Conversion range: 0 to VDDA)



Comparators (COMPx)

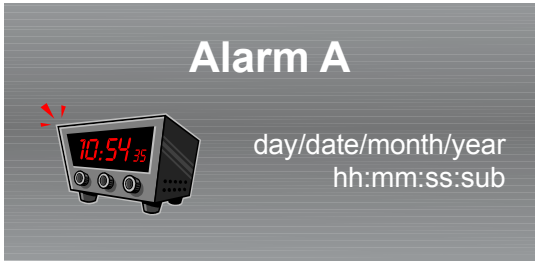
- 2 general purpose comparators with **rail-to-rail inputs**
- Programmable speed / consumption
- All I/Os **including outputs** are available
  - → **Can be used as standalone devices**
- Can be combined into a **window comparator**
- Multiple choices for threshold and output redirection
- Can be used for:
  - Exiting low power modes on analog event
  - Signal conditioning
  - Cycle-by-cycle current control (w/ DAC and TIM)
  - …

Timers (TIMx)

Timer	Width & Direction	CAPCOM + COMPL.	Prescaler & Max clock	DMA features	Synch. Module	External trigger	Break	Repetition counter
TIM1	16bit UP/DOWN	4 + **3**		All	Yes	Yes	Yes	Yes
TIM2	**32bit** UP/DOWN	4 + 0		All	Yes	Yes	No	No
TIM3	16bit UP/DOWN	4 + 0		All	Yes	Yes	No	No
TIM6	16bit UP only	0	Linear 16-bit	1 DMA req.	Yes	No	No	No
TIM14	16bit UP only	1 + 0	48 MHz	No	No	Yes LSE	No	No
TIM15	16bit UP only	2 + 1		All	Yes	No	Yes	Yes
TIM16	16bit UP only	1 + 1		All	No	No	Yes	Yes
TIM17	16bit UP only	1 + 1		All	No	No	Yes	Yes

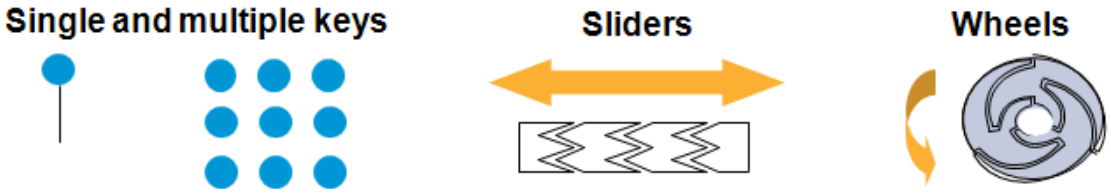
Real Time Clock (RTC)

- Ultra-low supply current **< 1uA** with RTC ON (MCU powered from VBAT)
- **Daylight saving** compensation programmable by software
- One programmable alarm (**Alarm A**), which can be triggered by any combination of the calendar fields
- A **reference clock source** (50 or 60Hz) can be used to update the calendar
- Time-stamp function for event saving with sub second precision (1 event)
- Digital **calibration circuit** (periodic counter correction) with 0.95 ppm res
- Maskable interrupts/events (Alarm A, Time-stamp,…)
- Clock sources: **LSE, LSI or HSE / 32**



Touch Sensing Controller (TSC)

- Proven and robust surface charge transfer acquisition principle
- Supports up to **18 capacitive sensing channels**
- Up to **6 capacitive sensing channels can be acquired in parallel** offering a very good response time
- **One sampling capacitor for up to 3 capacitive sensing channels** to reduce the system components
- **Spread spectrum** feature to improve system robustness in noisy environment
- Designed to operate with **STMTouch touch sensing firmware library**
- Compatible with **proximity**, **touchkey**, **linear** and **rotary** touch sensor implementation



Watchdogs (IWDG / WWDG)

- **Window Watchdog (WWDG)**
  - Configurable Time Window
  - Can detect abnormally early or late application behavior
  - Conditional Reset
  - WWDG Reset flag
  - Timeout value @48MHz: ***85.33us … 43.69ms***

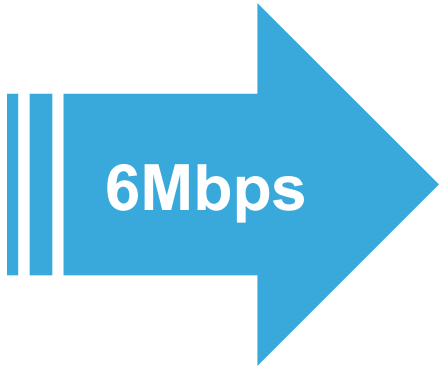
- **Independent Watchdog (IWDG) → IWWDG**
  - Dedicated low speed clock (LSI)
  - IWDG clock still active if main clock fails
  - HW and SW way of enabling
  - Still functional in Stop/Standby
  - Wake-up from stop/standby
  - IWDG Reset flag
  - **Window Functionality**
  - Timeout values @40KHz (LSI): ***100us …26.2s***

Universal Sync-Async Receiver Transmitter (USART)

Frame
- 8, 9 DATA bits
- 1, 1.5, 2 STOP bits
- Even, odd, none PARITY
- Oversampling /8 and /16 (default)

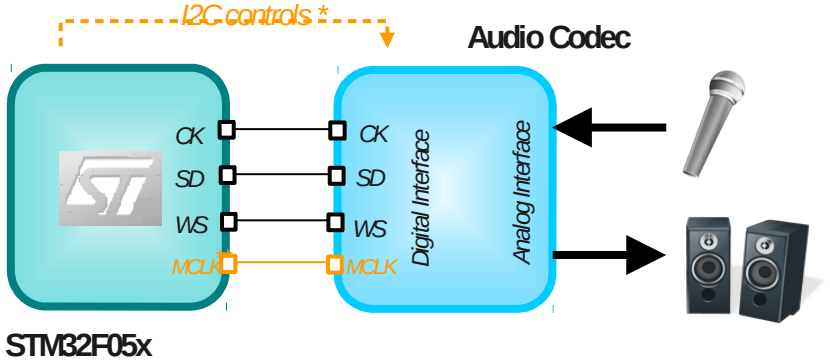
Modes
- Asynchronous
  - LIN
  - **SmartCard** (T=0, **T=1**)
  - IrDA
  - Basic **MODBUS**
  - Multiprocessor communication
  - Half duplex
- Synchronous (CLK line)

Other
- DMA support
- HW flow control (RTS, CTS lines)
- **Auto baudrate detection**
- Programmable data order (MSB/LSB)
- **Swappable Tx/RX pins**
- **Wakeup from STOP (!!! no data loss !!!)**



Serial Peripheral Interface / Inter-IC Sound (SPI / I2S)

- **SPI**
  - MASTER or SLAVE operation
  - Full-duplex (3w), half-duplex (2w) or simplex synchronous transfers (2 wires, unidirectional data line)
  - 4-bit to 16-bit data size selection, Two 32-bit embedded Rx and Tx **FIFOs**
  - Multimaster mode capability, **Daisy-Chaining** supported by HW
  - NSS management by HW or SW
  - SPI Motorola support
  - **CRC calculation** and check for reliable communication
- **I2S**
  - **Up to 192kHz, 32-bit**
  - I2S Philips
  - Left-Justified / Right-Justified
  - PCM standard



Inter-Integrated Circuit Interface (I2C)

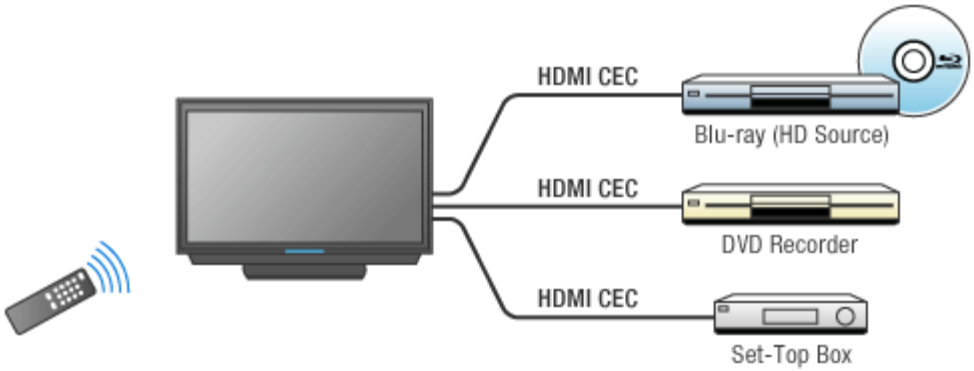
- **I2C Version 3.0** compatibility
- Slave and master modes with multimaster capability
- Standard-Mode, Fast-Mode and **Fast-Mode plus** (up to **1 MHz**)
- 7-bit and 10-bit addressing mode, multiple 7-bit slave addresses
- **Wakeup from STOP** on address match
- Programmable setup and hold times, optional clock stretching
- Easy to use event management, 1-byte buffer with DMA capability
- Programmable analog and digital **noise filters**
- SMBus ver. 2.0 and PMBus ver 1.1 standards compatibility

Infrared Interface (IRTIM)

- Can be used with an IR LED to perform **remote control functions**
- All standard IR pulse modulation modes can be obtained by programming the **two special timers** (TIM16 and TIM17)
- TIM16 used to generate the high frequency carrier signal, while TIM17 generates the modulation envelope
- The infrared function is output on the TIM_IR pin
- The **high sink LED driver capability** can be activated to sink the high current needed to directly control an infrared LED

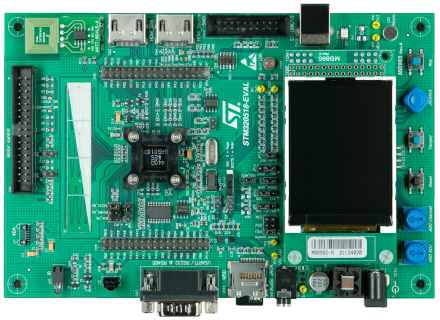
HDMI-CEC Controller (HDMI-CEC)

- Complies with **HDMI-CEC v1.4** specification
- **Works in STOP mode** for ultra-low-power applications
- A full free CEC firmware implementation provided as a part of STM320518-EVAL utilities firmware package – part of the Standard Peripheral Library



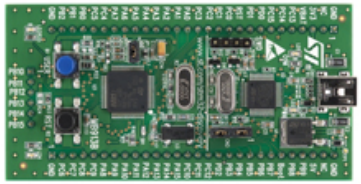
Extensive Tools and SW

- Evaluation board for full product feature evaluation
  - Hardware evaluation platform for all interfaces
  - Possible connection to all I/Os and all peripherals



STM320518-EVAL

- Discovery kit for cost-effective evaluation and prototyping



STM32F0DISCOVERY
$7.99

- Large choice of development IDE solutions from the STM32 and ARM ecosystem

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hitex DEVELOPMENT TOOLS
IAR SYSTEMS
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iSYSTEM
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TASKING
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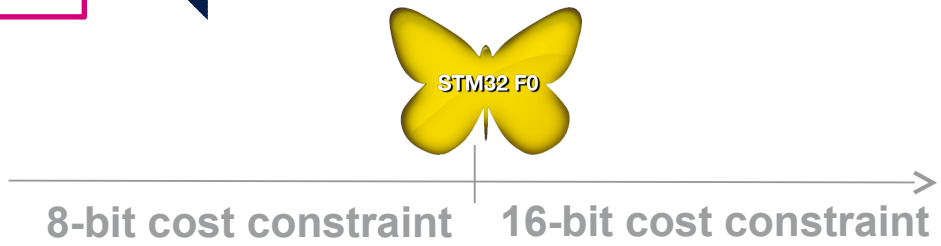
Speeds Up Cost-Constrained Decisions

Cutting cost often implies performance or platform headaches

Price positioning



- Save decision time:
  - No compromise on product performance
  - Wide STM32 platform benefit
  - Developers can re-use STM32F0 investment for future applications

 Budget price

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